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Docket No.: Bays 10-8-2
[D8143-00206] 4/3/03

MAR 2 6 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: El-Kik et al.

Examiner: David J. Huisman

Serial No.: 09/478,714

Group Art Unit: 2183

Filed: January 6, 2000

For: PROCESSOR SYSTEM INCLUDING INTERNAL ADDRESS GENERATOR FOR IMPLEMENTING SINGLE AND BURST DATA TRANSFERS

I, PATRICIA A. MCINTOSH HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 C.F.R. 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 2023.1.

on March 26, 2003

EXPRESS MAIL LABEL154823921US

PATRIGIA A. MCINTOSH

Assistant Commissioner for Patents

Washington, DC 20231

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Technology Center 2100

Sir:

PRELIMINARY AMENDMENT

Preliminary to an examination on the merits, please enter the following remarks and amendments:

In The Specification:

At page 5, lines 18-19, please delete the sentence beginning with "For a read operation..." and replace it with the following:

-- For a read operation, a RDN signal 135 is provided by chip select/internal address generator to the memory 125. —

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